Exhibit D-Part 2

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

EMC CORPORATION,

Petitioner,

v.

ACQIS LLC,

Patent Owner.

_____

Case IPR2014-01462 (Patent 8,041,873 B2)

Case IPR2014-01469 (Patent RE42,814 E)

Friday, August 28, 2015

Volume II of II

Deposition of VOLKER LINDENSTRUTH, taken at the offices of Gibson, Dunn & Crutcher, Carmelite House, 50 Victoria Embankment, London EC4Y 0DZ, beginning at 8:57 a.m. before Audrey Shirley, QRR, ACR, MBIVR.

A P P E A R A N C E S

FOR THE PETITIONER

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I N D E X

E X H I B I T S

(No exhibits were marked for identification.)

VOLKER LINDENSTRUTH, having been previously sworn, was examined and testified as follows:

EXAMINATION

BY MR. BUROKER:

Q. Good morning, Dr. Lindenstruth. 08:57:21

If you could pull out your copy of the '814 Patent, please from the stack of materials there. 08:57:25 08:57:29

A. Yeah. 08:57:33

Q. Okay? If you could look at Figure 18. 08:57:34 08:57:37

A. Yes. 08:57:44

Q. Did you review this figure in connection with your work on this case? 08:57:44 08:57:48

A. Sure. 08:57:49

Q. And looking at Figure 18, does it show a northbridge in that figure? 08:57:50 08:57:57

A. Well in the upper part of this diagram it's labeled "1805", it says "Integrated Host Interface [Controller] & North Bridge". 08:58:05 08:58:07 08:58:11

Q. And would that northbridge communicate address and data bits of PCI bus transaction? 08:58:15 08:58:17 08:58:22

A. Well, from this figure it is not directly shown. 08:58:24 08:58:28

Q. And if you could just quickly look at the '873 Patent and confirm that Figure 8 of the '873 Patent is the same as Figure 18 from the '814 Patent. 08:58:32 08:58:38 08:58:45 08:58:50

A. It has a different numbering, but that shouldn't ... 08:58:53 08:58:55

Q. That's true, let me rephrase that. 08:58:58

Is it true that the elements shown in Figure 8 of the '873 Patent are the same as the elements in Figure 18 of the '814 Patent, although the numbering has been changed from 805 and 810 to 1805 and 1810? 08:59:01 08:59:05 08:59:09 08:59:13 08:59:15

A. Yes, correct, I can confirm. 08:59:19

Q. Okay. And now I want to ask you some questions about again what we called the Bogaerts report, the status report of the RD24. I put a copy of that in front of you, that's Exhibit 1011 from the 814 Inter Partes Review proceedings. 08:59:24 08:59:28 08:59:34 08:59:39 08:59:41 08:59:55

So you gave some opinion in this case regarding claim 31 of the '814 relative to Bogaerts, correct? 08:59:55 08:59:57 09:00:02

A. Yeah. 09:00:03

Q. And Bogaerts was only instituted by the Patent Office with respect to claims 31 09:00:04 09:00:06

and a few of the depending claims, 31 and 33, is that your understanding? 09:00:11 09:00:18

A. Well, I believe I outlined that in my declaration. 09:00:19 09:00:21

Q. Yeah, and if you'd look at your '814 declaration, page 97 is at least one place to look. 09:00:23 09:00:28 09:00:31

A. Yeah, but didn't I say in the beginning which claims were -- yeah, exactly Institution Decision page 13. I believe I have it summarized there just to be -- yeah, exactly claims 24, 31 to 33, grounds: obvious over Horst, Mathers, and the LVDS Owners' Manual (Ground 1) and 31 through 33, obvious over Bogaerts, Gulick -- I hope I've pronounced that correctly -- Mathers and James (Ground 2). 09:00:47 09:00:49 09:00:54 09:00:57 09:01:01 09:01:03 09:01:06 09:01:06 09:01:11

Q. So the only claims on which the PTO instituted Inter Partes Review based on Bogaerts as a primary reference is 31 to 33; is that right? 09:01:14 09:01:22 09:01:26 09:01:29

A. Yes. 09:01:31

Q. Okay. And then on page 97 -- and probably perhaps other places in the declaration -- but at least starting on page 97 in your declaration you give some thoughts on why you 09:01:33 09:01:37 09:01:39 09:01:43

believe Bogaerts, Gulick -- I'm not sure how to pronounce it either -- Mathers and James don't disclose all of the limitations of 31 to 33, correct? 09:01:45 09:01:48 09:01:51 09:01:54

A. Uh-huh, yes. 09:01:55

Q. Okay. And at least one reason you've given, and it may be the only reason with regard to Bogaerts, is the subsection (a) that starts on 98, that you don't believe Bogaerts discloses to peripheral bridge to communicate address and data bits of PCI bus transaction in serial form, correct? 09:01:56 09:01:57 09:02:00 09:02:04 09:02:08 09:02:11 09:02:15

A. I'm just trying to ... 09:02:16

Q. Sure. 09:02:19

A. This is a longer section. Yeah, section 156 I think makes that clear: 09:02:20 09:02:37

"As a result, no PCI standard address or bus command is encoded into the serial SCI transaction or sent across the serial SCI ring." 09:02:40 09:02:42 09:02:45

And then I go further into what the PCI-SCI adapter would have to do. 09:02:49 09:02:52

Q. Right, okay. And the first figure you've shown there is Figure 15 from the Bogaerts reference, right? 09:02:57 09:03:07 09:03:12

A. Yes, on page 98. 09:03:15

Q. And yesterday you were asked questions about the PCI-SCI adapter. The PCI-SCI adapter that's discussed in Figure 15 is the Dolphin adapter not the adapter you developed; is that right? 09:03:17 09:03:18 09:03:26 09:03:30 09:03:37

A. At the instruction level of this document it's not said, but that I have to check in the RD24 report whether this is in the context of the other adapter. But, in general, if this is a PCI-SCI adapter both should work, right? 09:03:37 09:03:39 09:03:45 09:03:48 09:03:52

Q. Meaning that, if somebody were to take this figure, you could use either adapter to make them work. Is that what you're saying? 09:03:55 09:03:58 09:04:03

A. Yes, with a few minor caveats. The Dolphin PCI-SCI adapter, for example, as also shown on page 12 of the RD24 reference, as you can see is a wheel PCI device with an edge card connector, and the box on the right here on Figure 15 on page 98 of my report is in the context of a VME interface, as I say it's a VME Pentium. And, for example, if you look at Figure 9 on page 13 of the RD24 report, you will see that these VME systems have a different form factor like PCs. So this is basically one PCB with two connectors which is vertically mounted 09:04:06 09:04:09 09:04:14 09:04:19 09:04:24 09:04:34 09:04:39 09:04:42 09:04:49 09:04:55 09:05:00 09:05:08

into a crate, unlike a computer where you have a motherboard inside a box and the PCB is mounted vertically with respect to the motherboard, here the PCI cards or the add-on cards are mounted as mezzanine cards right on top of that board, which is sketched here, and this is why they are being called PCI mezzanine cards. There is an add-on to the PCI standard defining the PCI mezzanine card which is basically only defining a new mechanical form factor and a new connector layout. But aside from that, the same thing. 09:05:16 09:05:19 09:05:22 09:05:26 09:05:30 09:05:33 09:05:36 09:05:40 09:05:43 09:05:47 09:05:50

So because you were asking, I am not sure nor aware that Dolphin was really planning on making a PMC version of their PCI-SCI adapter, while the PCI-SCI adapter I built, and which is disclosed in here, was specifically built for this kind of framework and, therefore, had the PCI mezzanine form factor. 09:05:53 09:05:55 09:05:59 09:06:05 09:06:09 09:06:12 09:06:19

Q. If you look on page 17 of this article, the Bogaerts, under the subheading 5.1, the second paragraph says: 09:06:20 09:06:22 09:06:29

"A desktop Intel PC was used to connect a VME module (VMIC 7587) via two prototype Dolphin PCI-SCI adapters which we had available." 09:06:33 09:06:37 09:06:44

And then below that is shown Figure 15. 09:06:47

A. Now, for the left one, no question, this is a desktop computer. For the right one, that would mean there must be a PMC version of that as well, okay. 09:06:51 09:06:53 09:06:55 09:07:05

Q. If you look at the next page under "Result", it says: 09:07:07 09:07:10

"The transparent access of PCI memory space via SCI works." 09:07:11 09:07:13

So it suggests that what they're showing in Figure 15 was something that they built and worked, doesn't it? 09:07:16 09:07:17 09:07:20

A. Correct. If it says so then it must be correct. 09:07:28 09:07:30

Q. I know you said yesterday that you saw various things that other people were working on, what's shown in Figure 15, the connection of an Intel Pentium to a VME Pentium via PCI-SCI adapters, did you ever see that configuration built at CERN when you were there? 09:07:32 09:07:33 09:07:37 09:07:39 09:07:46 09:07:49

A. We discussed this yesterday and I'm quite sure I have seen it, but I have not worked on this particular setup. 09:07:51 09:07:53 09:07:57

Q. So you may have physically seen it but not investigated it to determine how it would work? 09:08:01 09:08:03 09:08:06

A. Right. I mean, my focus was on building the other PCI-SCI adapter, which is referenced here, I believe, as the CERN PCI-SCI adapter. 09:08:06 09:08:08 09:08:13 09:08:17

Q. So in the configuration of Figure 15, your declaration suggests that the PCI-SCI adapter would discard the PCI address and command information to create an SCI, I don't know if it's called a packet or a transmission? 09:08:17 09:08:19 09:08:27 09:08:31 09:08:36

A. Packet, or a set of packets. 09:08:38

Q. Okay, or a set of packets. 09:08:40

So how would the receiving PCI-SCI adapter know what command to execute and what address to use in this configuration of Figure 15 using the Dolphin PCI-SCI adapter? 09:08:43 09:08:48 09:08:52 09:08:57

A. I mean this brings us back to the discussion we had yesterday already about how does a PCI-TNet interface know what to do in case a TNet packet arrives. Same arguments hold to here. Basically what we have in between is an established network standard, in this case SCI. So for the PCI interface being a target, being addressed for some SCI packets it is entirely irrelevant who is the initiator of that packet, it could be any node, it could be any bus 09:09:01 09:09:03 09:09:06 09:09:13 09:09:16 09:09:23 09:09:26 09:09:31 09:09:36 09:09:38

behind it, it doesn't matter at all. Basically it receives SCI packets which has a certain command set set forth by the SCI standard and it does include reading and writing. There is a lot of functionality in SCI which cannot be executed on PCI for example, which would be the cache coherency functionality, so that would be responded as an error. 09:09:40 09:09:42 09:09:47 09:09:50 09:09:54 09:09:58 09:10:01 09:10:05

Now what particular command to be executed depends on the preset configuration of the PCI-SCI adapter which would have to be done beforehand. Also the configuration of the chips of the peripheral devices connected to that PCI bus -- because it doesn't make much sense talking to an empty bus -- would have to be done beforehand through some mechanism which is unspecified here. 09:10:06 09:10:08 09:10:12 09:10:15 09:10:22 09:10:25 09:10:28 09:10:33 09:10:35

Q. I'm not sure that answered my question. 09:10:39 09:10:41

So your answer is you don't know, that this does not explain how the SCI -- yeah, so let's just assume you went from right to left, the VME Pentium was sending something over to the Intel Pentium, the PCI-SCI adapter on the left, how would it know what command to execute and 09:10:47 09:10:50 09:11:01 09:11:04 09:11:08 09:11:12

what address to send the whatever command, 09:11:16
whether it was a read or write request, which 09:11:22
address to send it to? 09:11:24
MR. DAVIS: Objection; asked and 09:11:28
answered. 09:11:29
MR. BUROKER: It wasn't answered. Go 09:11:31
ahead. 09:11:32
MR. DAVIS: I disagree, it was 09:11:32
answered -- if you look at it, it's in there -- 09:11:34
but Dr. Lindenstruth can answer the question 09:11:35
again. 09:11:38
THE WITNESS: Let's say we receive 09:11:42
a write packet, you seem to prefer write packets. 09:11:49
So there is an SCI target address in this write 09:11:53
packet and an SCI subaddress space, which is 09:11:58
48 bits, which is meant to be used by the target 09:12:05
node for addressing the exact resources. There 09:12:09
is a length word, there are SCI commands, there 09:12:13
is a set of different possible packet formats 09:12:17
which SCI supports, these are 16 bits, 64 and 256 09:12:22
bytes, but 256 were not implemented here, that I 09:12:25
know. And now the PCI-SCI adapter has to 09:12:29
implement, like on TNet, an address translation 09:12:33
to convert that SCI address into a PCI address. 09:12:38
Then it would issue a PCI bus cycle which 09:12:43

particular to be used would have to be pre-configured. In the most common case it would most likely be an ordinary memory write transaction, but that is not automatically given. Usually there are some configuration registers inside that PCI-SCI interface which determined that then, so it's basically the context already pre-configured inside the adapter. Then it would issue the write transaction against its bus and perform the write request. 09:12:48 09:12:52 09:12:54 09:12:57 09:13:04 09:13:09 09:13:13 09:13:16 09:13:19 09:13:24

BY MR. BUROKER: 09:13:27

Q. Right. But in this particular, very specific configuration, why would it make any sense to throw away the PCI address and command information if you know it's going to be received by a PCI device which can interpret that information? It doesn't make any sense, does it? 09:13:27 09:13:30 09:13:34 09:13:40 09:13:44 09:13:47

A. I mean, what you are trying to build here is a modified SCI system for a very particular limited subset. And we discussed it yesterday also, what we have here is an interface which tries to allow communication between different predefined and set standards. Let's assume it was easily possible, what you say -- which I dispute, but let's just assume -- then we 09:13:51 09:13:58 09:14:06 09:14:09 09:14:15 09:14:18 09:14:25 09:14:29

have built something which only works if there is a PCI interface on the other side. But in most cases and systems envisioned here that would not be the case, right? So one of the ideas for SCI was that the processors would eventually adopt SCI as part of that internal communication scheme and the processors would start straight SCI as some sort of a replacement of the front side bus, and if you look at what Intel and AMD are doing today, there are intercommunication protocols between the different sockets which you have in a multi-socket node, and you look in detail, you will find that this has a lot of similarity to SCI, they have borrowed a lot of ideas there and AMD is extremely close. So the idea behind that was SCI is being an established standard and for the receiving node, the PCI-to-SCI interface, it couldn't make any assumption what was the agent type sending those packets and PCI was -- this is just one possibility, but it's only one of many and it would limit the utility of that device, so nobody would really do that. 09:14:32 09:14:33 09:14:36 09:14:41 09:14:45 09:14:48 09:14:50 09:14:53 09:14:56 09:15:01 09:15:04 09:15:05 09:15:09 09:15:12 09:15:14 09:15:17 09:15:22 09:15:26 09:15:29 09:15:32 09:15:35 09:15:38

Q. Well, but your analysis is based on your statement that this adapter would discard the address and command information, and that's 09:15:42 09:15:45 09:15:50

what your PCI-SCI adapter you testified did, correct? 09:15:53 09:15:57

A. Exactly. 09:15:58

Q. Do you know for sure that the Dolphin adapter did? 09:15:58 09:16:00

A. You have to have an address translation in order to couple those systems. 09:16:02 09:16:04

Q. But couldn't you keep the address and command information from the PCI bus transaction intact as part of your SCI packet as part of the payload and add an SCI address and not discard the PCI address and command information? 09:16:05 09:16:08 09:16:11 09:16:16 09:16:20 09:16:23

MR. DAVIS: Objection; form. 09:16:27

MR. BUROKER: That's possible, right? 09:16:27

MR. DAVIS: Objection; form. 09:16:33

THE WITNESS: You have different systems here which have different PCI buses where the PCI buses are initialized unilaterally by those nodes. So the left node would initialize its local PCI bus via the left processor in this context, and the right PCI bus would be initialized by the right CPU. SCI has no concept for initializing PCI segments, it's just not part of the standard. So that means the address maps 09:16:34 09:16:36 09:16:41 09:16:42 09:16:44 09:16:49 09:16:53 09:16:58 09:17:02

on either side in this diagram would be radically different as these are different computers: different hardware, different configurations, different devices plugged in. Consequently, since these address maps are different, you cannot assume that your address windows, which you try to address on the target node, are available address windows in the sending node, right? 09:17:03 09:17:08 09:17:11 09:17:13 09:17:17 09:17:20 09:17:24 09:17:27 09:17:32

BY MR. BUROKER: 09:17:32

Q. You're just explaining why you think there would be problems, but my question was: it's possible to include the packet in its entirety, the PCI bus transaction in its entirety in the SCI packet and add SCI address information, correct? 09:17:32 09:17:34 09:17:37 09:17:41 09:17:44 09:17:48

MR. DAVIS: Object to form. Asked and answered. 09:17:49 09:17:53

THE WITNESS: I mean we're extremely hypothetical here. I don't see that this would solve any of the technological problems we're discussing here, let alone that it makes any sense. 09:17:56 09:17:58 09:18:05 09:18:10 09:18:12

BY MR. BUROKER: 09:18:14

Q. So look at the next page, the 09:18:14

result page, it says under "Result", the second sentence: 09:18:16 09:18:21

"Memory on the PCI bus of the other modules can be seen after initialization of the access windows in the PCI configuration space." 09:18:21 09:18:25 09:18:27

Do you read that as meaning that only the PCI devices on one side of the SCI ring can be seen, or do you read that as suggesting that the PCI bus on one side of the SCI ring can read the memory of other modules across the SCI ring? 09:18:32 09:18:35 09:18:39 09:18:43 09:18:49

MR. DAVIS: Object to form. 09:18:56

THE WITNESS: Now, that was a long question. 09:18:58 09:18:59

BY MR. BUROKER: 09:19:00

Q. Well I'll shorten it, what do you think that sentence means? 09:19:01 09:19:02

MR. DAVIS: Object to form. 09:19:05

THE WITNESS: Basically this is another form of formulating the term "transparent access", right? One of the functionality sets of SCI and, in fact also TNet, is enabling direct read and write transactions to a remote node, to a remote target address inside that remote node which means after proper initialization the requesting agent -- I avoid the word "processor" 09:19:08 09:19:11 09:19:15 09:19:23 09:19:29 09:19:34 09:19:39 09:19:43

now because it could be a DMA engine as well -- can issue read or a write transaction on its local bus and through all this translation and packetizing, depacketizing and address translation business, eventually this transaction falls out at the far end to being executed. This is what this says, "after proper initialization". 09:19:47 09:19:52 09:19:57 09:20:03 09:20:08 09:20:11 09:20:15

BY MR. BUROKER: 09:20:18

Q. I just want to clarify one additional point. Do you know whether or not the Dolphin PCI-SCI adapter -- strike that. 09:20:18 09:20:21 09:20:26

Do you know how the Dolphin PCI-SCI adapter translated an address for the SCI packet from the PCI bus transaction it received? 09:20:31 09:20:39 09:20:45

A. I don't have the user manual of that device anymore, that's a long time ago. There was some mechanism but the details I don't remember. 09:20:47 09:20:49 09:20:52 09:20:54

Q. And you've talked about some problems that might be involved with the address in the information because on two sides of this SCI ring the PCI buses might use different addressing schemes, but PCI has standard commands, right? 09:20:55 09:21:00 09:21:06 09:21:09 09:21:13 09:21:16

A. Yeah. 09:21:17

Q. So why would the SCI interface throw out the command? It makes no sense, if it knows the PCI device is going to receive the command, that receiving PCI device will certainly know how to interpret the command, right? 09:21:18 09:21:23 09:21:28 09:21:30 09:21:32

MR. DAVIS: Object to form. 09:21:34

THE WITNESS: There are quite a few reasons, let me give you one example. And this is explained best at the example of a read transaction. There is a fundamental difference between what is happening inside the PCI bus and on the network, on basically any network. When the PCI transaction starts the initiator opens and says, "I want to do this". There is absolutely no indication in this moment as to how long the transaction will be, like how many words or bytes do I want to read now. So, if you now were to try to implement a, let me say, rather stupid and simple interface, where you say, "Okay, I have a read transaction, I send the read command for one word, maybe just one byte, depending on the byte enables, out to the target node, I get my byte back and I respond to the initiator." Take into account that both TNet and SCI had transaction latencies in the order of 09:21:39 09:21:42 09:21:48 09:21:51 09:21:57 09:22:01 09:22:04 09:22:09 09:22:11 09:22:16 09:22:19 09:22:25 09:22:30 09:22:33 09:22:36 09:22:40 09:22:43 09:22:50 09:22:53

microseconds, let's say half a microsecond, close to a microsecond, something like that, depending on scale. But unfortunately the initiator wanted to read more than one word, now it wants to read the next word by keeping its frame signal low. So again we would send a packet saying, "Please read the next word", come back and I answer. The performance you get out will be several orders of magnitude slower than if you would read from a local address inside the PCI bus. It would be so slow that it would be completely useless. So in order to make this work at any kind of a performance a lot of side effects had to be used and were used, and one of them is that we did, what we would call in this context, speculative read-ahead. So, we would make a guess and that, again, is depending on configuration and errors windows which could have their private particular configuration, we would say, "Well, what we have here is we are living inside a framework of a particular processor and at that time this particular processor had a cache line size of 32 bytes, so the most likely block length of a read would be 32 bytes" and if the address would match such a block read then we

09:22:56 09:23:00 09:23:01 09:23:04 09:23:07 09:23:12 09:23:14 09:23:17 09:23:20 09:23:24 09:23:26 09:23:31 09:23:33 09:23:36 09:23:43 09:23:45 09:23:49 09:23:53 09:23:55 09:23:57 09:24:01 09:24:05 09:24:07 09:24:10 09:24:14

would turn this whole read right at the beginning into a 32-byte read for the target node, pull all the 32 bytes back, then answer the first byte or the first word and see what happens. Next thing one would done is one would even keep the result, if the transaction ended premature, not reading everything, just in case the processor would come back soon later wanting another part out of those 32 bytes. 09:24:17 09:24:20 09:24:24 09:24:30 09:24:34 09:24:36 09:24:39 09:24:42 09:24:47

Another thing which was common practice then and certainly today, and it's being done more and more with I/O adapters, is to say, "Well how aggressive do I want to be reading ahead? Should I read another 32 bytes? Even 256 bytes? What would be a good optimum?" in order to avoid this initial load-stall, as we call it, when the processor has to wait for the first word to come back. 09:24:48 09:24:51 09:24:53 09:24:57 09:25:00 09:25:04 09:25:08 09:25:11 09:25:13

Take into account that, I mean, at that time processors were clocked at something like couple of hundred megahertz, which means if you have a delay to respond, let's say, of the scale of one microsecond, the processor was basically wasting time corresponding to hundreds of instructions which is a huge waste, which 09:25:15 09:25:19 09:25:21 09:25:28 09:25:31 09:25:36 09:25:38

shouldn't happen at all. There are latency hiding tricks, but once you get into that stall, you have that problem. So there is a good reason why you even would not want to just send over such a highly complex and comparably much, much slower network, right? I mean the Acqis case is something completely different, there they specify latencies of the order of one and a half, two clocks. Here we specify latencies in the order of hundreds of clocks, to kind of mitigate that unavoidable disadvantage of these larger systems to have very intelligent and optimum way of reacting to the local PCI transaction. 09:25:41 09:25:43 09:25:46 09:25:50 09:25:54 09:25:58 09:26:01 09:26:03 09:26:06 09:26:09 09:26:11 09:26:15 09:26:18

BY MR. BUROKER: 09:26:29

Q. Well, do you acknowledge that in what's shown in Figure 15, whatever PCI bus transaction command is received by one of the adapters, there's going to be a command in the SCI packet that's based on the command in the PCI bus transaction? 09:26:29 09:26:35 09:26:39 09:26:42 09:26:50 09:26:59

MR. DAVIS: Object to form. 09:26:59

BY MR. BUROKER: 09:27:00

Q. So, let me start again. If the PCI bus transaction coming into the adapter is a read transaction, the PCI-SCI adapter, you're 09:27:00 09:27:02 09:27:05

saying, will throw away the PCI bus command and insert some other command, right? 09:27:12 09:27:19

A. Yes. 09:27:22

Q. And that command is based on what was in the PCI bus transaction command? 09:27:22 09:27:24

MR. DAVIS: Objection to form. 09:27:27

BY MR. BUROKER: 09:27:29

Q. Right? 09:27:29

A. A read would not translate into a write at first, yes. But there are choices which particular read to be used and that, in a good adapter, will change over time and context, load of the system, availability of internal storage and so forth. 09:27:29 09:27:31 09:27:34 09:27:39 09:27:42 09:27:46

Q. Okay, right. So then the receiving PCI-SCI adapter in this configuration receives the SCI packet, how does it know what PCI bus transaction command to use based on what's in the SCI packet? 09:27:48 09:27:50 09:27:54 09:27:59 09:28:05

A. That would be pre-configured and there is only a limited amount of playground you have here. But one example, I mean the simplest way would be to turn it into a generic read. 09:28:07 09:28:15 09:28:17 09:28:22

Q. So a read PCI transaction command would be translated by the SCI-PCI adapter into 09:28:25 09:28:30

an SCI read command and then on the receiving end would be translated back by the receiving PCI-SCI adapter into a PCI read transaction; is that correct? 09:28:37 09:28:41 09:28:47 09:28:51

MR. DAVIS: Object to form. 09:28:52

THE WITNESS: Or possibly multiple read transactions in order to implement all that performance-enhancement functionality, yes. 09:28:53 09:28:56 09:28:58

BY MR. BUROKER: 09:29:00

Q. And where would the multiple read transactions be, in the receiving PCI bus transaction or in the SCI packet? 09:29:01 09:29:03 09:29:06

A. I mean typically there would be multiple such packets submitted by the initiating device in your example on the right side, and they would be then worked one after the other by the target device. The target device wouldn't know what is behind it. It would just see here's a transaction, it does its thing, there's the next one, it does its thing, and so it proceeds. 09:29:11 09:29:13 09:29:18 09:29:22 09:29:24 09:29:28 09:29:30 09:29:32

Q. And we talked yesterday about TNet but I'm not sure I asked you this. Is the data part of the PCI bus transaction, is anything done to that or is it just placed in the SCI packet, one or more SCI packets depending on size? 09:29:39 09:29:41 09:29:44 09:29:51 09:29:57

MR. DAVIS: Object to form. 09:29:59

BY MR. BUROKER: 09:30:01

Q. By the PCI-SCI adapter in 09:30:02

Figure 15, for example? 09:30:05

MR. DAVIS: Object to form. 09:30:06

THE WITNESS: In case of TNet I believe 09:30:08

I remember I said yesterday it is encoded, they 09:30:11

have this 8B/9B encoding. 09:30:15

In case of SCI, I know this quite well, 09:30:18

but now I would really take a look, so this has 09:30:23

to be taken with a grain of salt, I'm relatively 09:30:27

sure that there is an 8B/10B encoder in there, 09:30:31

but that I'm not 100 percent positive. 09:30:35

BY MR. BUROKER: 09:30:37

Q. That would be after the packet was 09:30:37

created, then it would be 8B/9B encoded before 09:30:38

transmission; is that correct? 09:30:42

A. I would now like to study the 09:30:46

diagram of the physical layer of an SCI interface 09:30:47

to be certain. 09:30:51

Q. And you're saying that diagram is 09:30:52

not in the Bogaerts reference? 09:30:55

A. No, this is in the SCI standard, 09:30:57

the 1596 standard which is a five or 600-page 09:30:59

document. 09:31:03

The reason why I'm relatively certain it would have to be done is this is done to implement AC balancing, I'm sure you know the game what is behind, which is needed to allow for the electrical interface to perform easily, so there is basically some reason for having it. But I don't want to speculate. So there may be some encoding similar to what was done in Bogaerts but with different parameters. 8B/10B encoding is a relatively simple thing. 09:31:04 09:31:07 09:31:10 09:31:13 09:31:17 09:31:23 09:31:27 09:31:30 09:31:35 09:31:39

Q. Just so I understand the process, the PCI bus transaction would be received by the adapter. Is an SCI packet created first and then your question is whether that SCI packet is encoded or not? Or is part of creating the packet potentially encoding? That's why I'm confused. What's your confusion? 09:31:42 09:31:44 09:31:47 09:31:55 09:31:58 09:32:00 09:32:04

MR. DAVIS: Objection to form. 09:32:07

THE WITNESS: I cannot give you a definitive answer off the top of my head, for that I would really like to look at the standard. We can do that, I believe it's on the net. I didn't bring my computer, I have it on it but we didn't print it out because it's so much paper. 09:32:09 09:32:12 09:32:14 09:32:17 09:32:21 09:32:26

/// 09:32:26

BY MR. BUROKER: 09:32:29

Q. All right. So then I wanted to 09:32:29

ask you some questions about this reference in 09:32:37

paragraph 155 and 156 of your '814 declaration. 09:32:42

I think you've got it open right in front of you 09:32:50

there. 09:32:53

A. 160, you said? 09:32:53

Q. No, it's on page 99. So actually 09:32:54

I want to ask you about paragraph 159. 09:33:33

A. Yeah. 09:33:37

Q. So there you're talking about the 09:33:38

peripheral bridge limitation of claim 31, and it 09:33:41

says: 09:33:45

"Bogaerts fails to disclose 09:33:45

a peripheral bridge that meets that limitation." 09:33:47

And you can read the limitation. So 09:33:49

you say that: 09:33:52

"... in Figure 15, the PCI-SCI adaptors 09:33:54

clearly have PCI busses intervening between the 09:33:58

CPU." 09:34:03

Do you see that? 09:34:03

A. Yeah. 09:34:04

Q. Okay. So you're looking at 09:34:04

Figure 15 and saying that the only thing that 09:34:08

could be a peripheral bus is the PCI-SCI adapter 09:34:11

and because there's a PCI bus shown in that both sides of the figure there, they can't meet the limitation of claim 31, is that correct? 09:34:17 09:34:23 09:34:27

A. Let me just look and pull out Figure 15 again. 09:34:31 09:34:37

Q. Page 17. 09:34:38

A. Absolutely right. In these diagrams any of the peripheral devices are connected through a PCI interface. 09:34:49 09:34:50 09:34:53

Q. Through a PCI bus? 09:35:01

A. Yeah, PCI bus. 09:35:03

Q. Okay. What is the box that says "PCI set"? 09:35:05 09:35:11

A. You mean in Figure 15? 09:35:15

Q. Yeah, it's on both sides of the... 09:35:17

A. I read this as the interface between the front side bus of the processor here sketched as "CPU", "Cache" and "Memory", in the right figure the word "Cache" was reduced to a simple "C". And "PCI set" is obviously in this context the bridge between the host CPU and PCI bus. In some cases it is also, I believe, called southbridge but here it's just the interface between the front side bus of the CPU and the PCI bus of that particular computer. 09:35:26 09:35:28 09:35:31 09:35:35 09:35:38 09:35:47 09:35:54 09:36:06 09:36:08 09:36:11

Q. In fact, if you look on page 22, under 6.1, this is discussing a different configuration, but it says in the second sentence: 09:36:12 09:36:17 09:36:24 09:36:26

"The two PCs are interconnected through Dolphin PCI-SCI Adapters are 133 [megahertz] Pentium processors with the Intel 430HX (Triton 2) PCI set ..." 09:36:26 09:36:29 09:36:34 09:36:40

So it's got the same name PCI set. It may be not the exact same PCI set, but are you familiar, what is an Intel 430HX Triton 2 PCI set? 09:36:41 09:36:46 09:36:49 09:36:55

A. That must be some version of a southbridge, but I don't know the particular features of that anymore, this is a long time ago. But as shown in these diagrams, it must be such a device. 09:36:55 09:36:57 09:37:00 09:37:04 09:37:08

Q. And that PCI set would be connected to the CPU cache and memory, that would be a CPU bridge -- excuse me, a CPU bus; is that correct? 09:37:10 09:37:13 09:37:17 09:37:21

MR. DAVIS: Object to form. 09:37:22

THE WITNESS: I mean the generic architecture of these systems usually had a northbridge which interfaced the CPU to the 09:37:28 09:37:32 09:37:35

memory and also had a high performance graphics interface and then some kind of intermediate bus -- which sometimes was and sometimes as not PCI -- to a southbridge, which would then connect the periphery and having one or several PCI buses. And I'm just trying to find, I believe I put a figure in here about this northbridge/southbridge architecture. 09:37:39 09:37:44 09:37:47 09:37:49 09:37:52 09:37:55 09:37:57 09:37:59

These diagrams are highly abstracted and I don't think that this chip would, as such, interface directly but that would have to be checked if this is of any importance. 09:38:02 09:38:04 09:38:10 09:38:13

BY MR. BUROKER: 09:38:16

Q. Which chip would have interfaced directly to the CPU? 09:38:16 09:38:18

A. The one you just quoted, the 430HX Triton 2 set. 09:38:19 09:38:27

Q. You don't think it would have interfaced directly to the CPU? 09:38:29 09:38:30

A. Yeah. 09:38:32

Q. Is that what you said? 09:38:33

A. (The witness nodded.) 09:38:38

Q. Okay. Well, in Figure 15 it shows the word "PCI bus" next to the line on the left, but it doesn't say "PCI bus" on the set of lines 09:38:39 09:38:45 09:38:50

between the "C", "CPU" and "M" on the one side and the "PCI set" on the other, correct? It doesn't say "PCI bus" over there? It just has it in one place. 09:38:55 09:38:58 09:39:01 09:39:05

A. "Over there"? You mean where it says "CPU bus"? I didn't see where you were pointing to. 09:39:06 09:39:08 09:39:15

Q. Oh yeah, this word "CPU bus" down there, you think that applies to this bus here between the "C", "CPU", "M" boxes and the "PCI set"? 09:39:16 09:39:21 09:39:25 09:39:30

A. I mean, this figure could be a bit more clear and could have a few more definitions in there to make it clearer. So, for example, that bus between the CPU and the PCI set as it is drawn here, could be labeled as such. Further, for example, the fact that this cache, which is obviously drawn in the context of the Pentium processor, is not a device which is connected to the front side bus, this is sitting between the processor and the front side bus in every computer and also every computer at that time, so this is a bit sloppy. The VME bridge has an interface drawing to VME but is not connected anywhere in here. But that happens if people 09:39:31 09:39:38 09:39:45 09:39:47 09:39:51 09:40:00 09:40:05 09:40:09 09:40:11 09:40:13 09:40:16 09:40:18 09:40:23 09:40:27

write documents for people who know this stuff inside out. And these VME bridges here, to the best of my knowledge, were interfacing also to PCI. 09:40:29 09:40:31 09:40:35 09:40:37

Q. Right, it should have connected to left-hand PCI bus, right? 09:40:38 09:40:40

A. Yeah. 09:40:41

Q. And so should be the LAN, the LAN box should be connected to the PCI box? 09:40:42 09:40:44

A. Exactly, the LAN box doesn't do anything here also, it's just standing there. It would definitely not be connected to the front side bus of the processor and in case of the PCI set, since it's called "set", to me it seems to be a chipset. Normally you acquire processors and then you acquire the chipset to do all the periphery and interfacing of these devices, and they are usually -- basically these two are sometimes also called northbridge/southbridge. But in this particular case this is too long ago, I don't remember the exact details of this Intel 4030HX PCI set. 09:40:47 09:40:48 09:40:51 09:40:54 09:40:56 09:40:59 09:41:03 09:41:08 09:41:13 09:41:17 09:41:19 09:41:22 09:41:26

Q. And did you consider as a possible peripheral bridge the combination of the PCI-SCI adapter and the PCI set? 09:41:28 09:41:31 09:41:36

A. Now in exactly what claim? 09:41:43

Q. In Figure 15. You've said the 09:41:45

only possible peripheral bridge in Figure 15 is 09:41:47

the PCI-SCI adapter. 09:41:52

A. Okay, wait a minute, I have now 09:42:01

lost my text. We were at page? 09:42:04

Q. Bottom of page 100 of your 09:42:08

declaration. 09:42:13

A. And we are talking about claim 31? 09:42:18

Q. Right. 09:42:21

A. In the '814. Right, I mean it 09:42:26

says: 09:42:59

"... peripheral bridge coupled to said 09:43:00

microprocessor unit without any intervening 09:43:02

Peripheral Component Interconnect (PCI) bus, said 09:43:04

peripheral bridge coupled to said second LVDS 09:43:07

channel to communicate ..." 09:43:10

-- and so forth: 09:43:10

"... address and data bits of PCI bus 09:43:13

transactions." 09:43:16

So, since you have the limitation of 09:43:17

having these LVDS links, in the context of 09:43:18

Bogaerts that end would have to be the SCI link, 09:43:26

right? 09:43:29

Q. Okay. 09:43:30

A. And then basically all the building blocks are based on a PCI-SCI adapter and then you have PCI in between. 09:43:32 09:43:39 09:43:42

Q. Right, but the peripheral bridge, if the peripheral bridge, the combination is one block that is the PCI-SCI adapter and the PCI set, on the one hand it would be connected to an LVDS channel, the SCI ring, right? 09:43:44 09:43:47 09:43:54 09:43:58 09:44:01

MR. DAVIS: Object to form. 09:44:07

THE WITNESS: So -- 09:44:11

BY MR. BUROKER: 09:44:13

Q. Let me just break it down. You agree that the PCI-SCI adapter is connected to the SCI ring which is a low-voltage differential signal channel, right? 09:44:13 09:44:15 09:44:17 09:44:23

A. Yes. 09:44:24

Q. And you agree that the PCI set is connected to the CPU? 09:44:25 09:44:29

A. Yes. 09:44:31

Q. And do you agree that that is not using a PCI bus? 09:44:31 09:44:38

MR. DAVIS: Object to form. 09:44:40

THE WITNESS: You mean the front side bus of the CPU? 09:44:42 09:44:43

/// 09:44:45

BY MR. BUROKER: 09:44:45

Q. Right, the connection between the 09:44:45

PCI set and the CPU? 09:44:49

MR. DAVIS: Object to form. 09:44:51

BY MR. BUROKER: 09:44:53

Q. Is that a PCI bus connection? 09:44:53

MR. DAVIS: Object to form. Asked and 09:44:56

answered. 09:44:58

MR. BUROKER: No, he didn't. 09:44:59

BY MR. BUROKER: 09:44:59

Q. Go ahead. 09:45:01

MR. DAVIS: He answered that question 09:45:03

earlier. 09:45:04

MR. BUROKER: No, he didn't. 09:45:05

BY MR. BUROKER: 09:45:05

Q. Go ahead. 09:45:06

MR. DAVIS: He did. He can answer it 09:45:07

again, but he answered it earlier. 09:45:08

BY MR. BUROKER: 09:45:11

Q. You can answer. 09:45:11

A. In this case the figure says that 09:45:15

there is a Pentium processor being used and the 09:45:18

Pentium processor has a front side bus which is 09:45:23

not PCI. 09:45:26

Q. Okay, so the connection between 09:45:31

PCI set to that front side bus would be some other kind of bus other than PCI, correct? 09:45:32 09:45:35

A. In the term of art it's called the front side bus, yes. It's a bus tuned for the highest possible performance because this is where the processor gets all its information from and you may have heard about memory bottleneck in all computers these days, so this is place where usually computers suffer performance-wise, and this is the place which is highly optimized, and a peripheral bus, like PCI, would not be the right thing to solve. 09:45:38 09:45:40 09:45:43 09:45:46 09:45:49 09:45:56 09:45:59 09:46:02 09:46:06 09:46:08

Q. So then you next look at Figure 13, and you say in paragraph 160: 09:46:12 09:46:33

"... the only system in Bogaerts that can be a peripheral bridge without an intervening PCI bus is found in Figure 13." 09:46:37 09:46:39 09:46:41

And you draw a red box around some of the components in the top-right section of Figure 13, right? 09:46:49 09:46:56 09:47:00

A. Yes. 09:47:04

Q. And those components that are in the red box on page 101 of your '814 declaration, would connect to one or more CPUs via a bus that's not a PCI bus. Is that your 09:47:12 09:47:15 09:47:19 09:47:22

interpretation? 09:47:24

A. If I take that in the context of 09:47:25
the reference we had at the time, then CPU what 09:47:29
is stated here would be something like a Pentium 09:47:35
CPU, or something similar from a different 09:47:38
vendor, and in that case this bus would not be 09:47:40
PCI. 09:47:44

Q. Right. And if you substituted, in 09:47:48
fact if you took what was either of the systems 09:47:51
shown in Figure 15, and plugged those into this 09:47:58
SCI architecture in Figure 13, you would have the 09:48:05
same thing. You would have CPUs that would be 09:48:09
connecting to various components using a non-PCI 09:48:14
bus, right? 09:48:18

MR. DAVIS: Object to form. 09:48:21

THE WITNESS: That I'm not sure I 09:48:22
understood. 09:48:24

BY MR. BUROKER: 09:48:25

Q. Well, never mind. You could use 09:48:25
the configurations shown in Figure 15 and connect 09:48:29
those configurations to this SCI ring shown in 09:48:34
Figure 13, couldn't you? 09:48:37

MR. DAVIS: Object to form. 09:48:39

THE WITNESS: SCI is an established 09:48:43
standard, so every SCI device compliant with that 09:48:44

standard can be connected to a larger SCI network with a large variety of different configurations. So, of course, one could take the SCI ring of Figure 15 and connect it to the SCI ring as shown in Figure 13 of the Bogaerts reference, certainly true. While I should say the ring here is only an oversimplification, of course, that is the same thing such as all the other functionality you have to have in a larger network. 09:48:48 09:48:53 09:48:57 09:49:00 09:49:07 09:49:11 09:49:14 09:49:17 09:49:20

BY MR. BUROKER: 09:49:20

Q. And so those components in Figure 15 could connect to an SCI ring which would then enable them to connect to a disk subsystem or an I/O expansion as shown in Figure 13, right? 09:49:25 09:49:29 09:49:31 09:49:35 09:49:40

MR. DAVIS: Object to form. 09:49:43

THE WITNESS: Every device connected to an SCI network can, contingent upon the correct setting of all the address mapping and access control and everything, proper initialization, in principle communicate with every other node, I mean this is the idea of such a network, and that includes particular I/O subsystems of any sort. 09:49:46 09:49:48 09:49:51 09:49:53 09:49:57 09:49:59 09:50:02

BY MR. BUROKER: 09:50:24

Q. And the reason why you say what 09:50:24

you've labeled here as the potential bridge doesn't transmit PCI bus transaction information is because at the PCI-SCI adapter the address and command information would be discarded and an SCI packet would be created; is that correct? 09:50:31 09:50:39 09:50:41 09:50:50 09:50:57

MR. DAVIS: Object to form. 09:51:00

THE WITNESS: Which particular signal flow are you discussing now? I'm a bit lost. 09:51:10 09:51:11

BY MR. BUROKER: 09:51:16

Q. I'm trying to understand your explanation in paragraph 160. 09:51:16 09:51:18

A. Okay. 09:51:20

Q. You say the peripheral bridge in Figure 13 that's connected directly to a microprocessor without any intervening PCI is what you put a red box around in the top right-hand side. 09:51:20 09:51:24 09:51:26 09:51:30 09:51:35

A. Right. 09:51:36

Q. Correct? 09:51:37

A. Correct. 09:51:38

Q. Okay. 09:51:38

A. Because link controller is one of the new devices which Dolphin had produced capable of generating SCI packets out of the front side bus of that particular chip and that 09:51:40 09:51:41 09:51:45 09:51:50

would have to be interfaced somehow to the memory and cache controller dealing with the CPUs. Whereas in this diagram the cache controller would have been to something like a level 3 cache controller which at that time was, indeed, external, but, yeah, that would be the functionality. 09:51:52 09:51:54 09:51:59 09:52:01 09:52:04 09:52:06 09:52:08

Q. Okay, and that is connected to an LVDS channel in the form of the SCI network? 09:52:10 09:52:12

A. Correct. 09:52:18

Q. Right. So then the part that you think is missing from that element of claim 31 is you don't believe it communicates address and data bits of PCI bus transaction in serial form, correct? 09:52:18 09:52:21 09:52:27 09:52:29 09:52:33

A. Yes. 09:52:33

Q. You disagree that it transmits something in serial form, which is the SCI packet, right? 09:52:34 09:52:36 09:52:40

A. Yes. 09:52:41

Q. It's just not address and data bits of PCI bus transaction, right? 09:52:41 09:52:45

A. Yes. 09:52:47

Q. Does it communicate data bits of PCI bus transaction? 09:52:47 09:52:52

MR. DAVIS: Object to form. 09:52:52

THE WITNESS: It transmits some data 09:53:04
which, depending on the configuration of the 09:53:07
system, and the target address of that packet, 09:53:09
may result finally in it being data as part of 09:53:12
a PCI transaction on the remote node. 09:53:21

BY MR. BUROKER: 09:53:27

Q. Okay. But you don't agree in any 09:53:27
-- strike that. 09:53:30

It's your opinion that a person of skill 09:53:33
in the art reading the Bogaerts reference would 09:53:36
understand that the address information of a bus 09:53:40
transaction, PCI bus transaction would be 09:53:47
discarded and therefore wouldn't be communicated 09:53:50
over the SCI network; is that correct? 09:53:52

A. That there would have to be 09:53:55
an appropriate set of address translations 09:53:58
implemented in order to enable such functionality 09:53:59
to work, yes. 09:54:01

But, I mean, I understand what you're 09:54:03
trying to get to, namely to say if there is 09:54:07
finally a PCI transaction there has to be some 09:54:11
content, some gist of it already present on the 09:54:14
originating node. And I mean very placative 09:54:19
I would say, if you submit a print job from your 09:54:27

computer and at the final end a document is being printed, the same arguments could hold true, arguing well the content on that paper somehow was or had to be already on the computer otherwise the printer couldn't have printed. But that doesn't allow the conclusion that the paper had to go through the network because at the final end paper came out, right? So, I mean, if the term says "data of a PCI bus transaction", and at the stage where this whole thing is initiated, packets generated and so forth, there is no context of a PCI transaction. In fact, after an initialization of that system, the particular program issuing such transaction doesn't even need to know whether or not this at the far end ends up being a PCI transaction or something else, or a VME transaction for that matter, totally irrelevant. I mean this is one of the powerful features of our system, that it allows to abstract away from that. 09:54:32 09:54:35 09:54:38 09:54:41 09:54:43 09:54:45 09:54:47 09:54:50 09:54:55 09:55:00 09:55:06 09:55:10 09:55:14 09:55:18 09:55:22 09:55:25 09:55:29 09:55:30 09:55:33 09:55:36

Q. In Figure 15 you I think agreed that the LAN would normally be understood to be connected to that PCI bus; is that correct? 09:55:49 09:56:02 09:56:06

A. Yes. 09:56:08

Q. So a transaction from the LAN, to 09:56:09

communicate back to the CPU the LAN would have to be able to create a PCI bus transaction on the PCI bus shown in Figure 15, right? 09:56:23 09:56:26 09:56:32

A. You mean the right portion of Figure 15? 09:56:36 09:56:39

Q. Right, the right-hand portion, the LAN there. 09:56:39 09:56:42

A. Agreed, for the missing link to this LAN interface. 09:56:43 09:56:45

Q. Assuming that there is a connection, that LAN would need to create a PCI bus transaction on the PCI bus to be able to communicate back with the VME Pentium CPU shown there, right? 09:56:46 09:56:48 09:56:51 09:56:55 09:57:00

A. Yes. 09:57:00

Q. And if that LAN wanted to communicate over to the Intel Pentium on the left-hand side, it would create a PCI bus transaction that would go on the PCI bus and the PCI-SCI adapter would then do its job and send something over the SCI ring, correct? 09:57:04 09:57:07 09:57:14 09:57:16 09:57:19 09:57:22

A. Yeah. For the arguments we have been using so far, it doesn't matter whether or not the LAN controller or the CPU initiates the PCI bus transaction. Basically the PCI-SCI 09:57:28 09:57:30 09:57:36 09:57:39

interface sees the PCI bus transaction. In fact, 09:57:46
PCI has no functionality to allow the target 09:57:48
device to identify who is the initiator of this, 09:57:52
it doesn't know who it is talking to. And if the 09:57:54
right addresses and all the pre-configuration is 09:57:59
done correctly then the PCI bus interface would 09:58:02
do its thing. However this is pretty much the 09:58:06
last thing one would want to do. 09:58:10
Q. The PCI-SCI adapter, it must have 09:58:12
its own address then on the PCI bus; is that 09:58:19
right? 09:58:23
A. Yeah. 09:58:23
Q. Okay. 09:58:24
A. It has an address window. So 09:58:25
normally the PCI-SCI adapter would present itself 09:58:26
as a bridge device which means it could have 09:58:33
a huge address space behind it. The amount of 09:58:37
address space inside the PCI address sometimes is 09:58:42
configurable, because, for example, in a 32-bit 09:58:47
PCI space it wouldn't make sense to present 09:58:50
a 4 gigabyte window because then you cannot have 09:58:56
any other PCI devices left, then there are no 09:58:58
addresses left. So we have a certain amount of 09:58:59
memory window which is configured in the 09:59:01
initialization phase of the computer, a base 09:59:07

address is assigned to this adapter, and if then the adapter sees a PCI transaction hitting any part of that window, it will have to start doing some of those things you have been discussing. What is often done is that different regions within this window can have different functionality being triggered; different address translations for these particular windows addressing different nodes and so forth. 09:59:09 09:59:12 09:59:16 09:59:20 09:59:24 09:59:27 09:59:30 09:59:34 09:59:37

Q. And on that PCI bus physical addressing is used, but then your contention is that once you are in the SCI domain virtual addressing is used, right? 09:59:45 09:59:49 09:59:53 10:00:00

MR. DAVIS: Object to form. 10:00:01

THE WITNESS: TNet likes to call them virtual addresses, I believe SCI just calls them SCI addresses which are something similar because there is no direct one-to-one relationship. The way I like to define physical addresses is that to every given particular physical address there is a one-to-one relationship of a particular device or nothing, right -- not every address has a device associated to it -- while all other addresses which are translated can have different meanings. 10:00:03 10:00:05 10:00:07 10:00:14 10:00:16 10:00:21 10:00:24 10:00:28 10:00:32 10:00:36 10:00:39

BY MR. BUROKER: 10:00:40

Q. And so an SCI address is a 64-bit address? 10:00:41 10:00:44

A. Yes. 10:00:45

Q. And it's your understanding that in your PCI-SCI adapter none of those 32 address bits from the PCI bus transaction were used to create the 64-bit SCI address; is that correct? 10:00:45 10:00:55 10:00:59 10:01:02

MR. DAVIS: Object to form. 10:01:08

THE WITNESS: We had the discussion about address translation yesterday where I tried to outline -- 10:01:09 10:01:11 10:01:14

BY MR. BUROKER: 10:01:15

Q. But yesterday we weren't talking about SCI, I'm asking specifically about your PCI-SCI adapter. So you're clear on the question: your PCI-SCI adapter, did it use the 32 bits from the address to create the 64-bit address? 10:01:15 10:01:17 10:01:20 10:01:22 10:01:26 10:01:29

MR. DAVIS: Object to form. 10:01:30

BY MR. BUROKER: 10:01:30

Q. I want to make sure the question was clear. 10:01:33 10:01:34

A. I understood the question. What I was trying to say is that basically every address 10:01:34 10:01:36

translation is based on certain pages and page numbers. It wouldn't make sense to translate the address of every individual byte because then the address translation table needs more space than the memory associated to that address, right? So there is always a set of some sort of paging. I would have to check, I believe I used also 4-kilobyte pages but there I'm not 100 percent sure, but it would make some sense to match it to the paging of a computer, which means the lower 12 bits of the PCI address would be transmitted unchanged. The higher bits would be the index into some sort of a lookup table, could be a multi-stage lookup table, to convert them into the SCI address being attached to that and then off it goes. So also the lower 12 bits of the virtual address of a processor are translated directly unchanged into the physical address and there are technical reasons for that, otherwise the address translation would dramatically slow down the CPU. 10:01:39 10:01:41 10:01:45 10:01:47 10:01:49 10:01:55 10:02:03 10:02:08 10:02:11 10:02:15 10:02:19 10:02:23 10:02:27 10:02:31 10:02:34 10:02:39 10:02:46 10:02:50 10:02:52 10:02:54 10:02:57

Q. And I think you said you are not sure how the Dolphin people created their SCI addresses from PCI bus address; is that correct? 10:02:58 10:03:02 10:03:10

A. Yes, I have not worked a lot with 10:03:13

this device, it wasn't my focus. And now this is a bit too long ago that I can remember these details. 10:03:17 10:03:21 10:03:24

Q. And there's a PRO-SCI device that's discussed this in document. You didn't work on that one either? 10:03:25 10:03:32 10:03:34

A. Let me just check quickly. 10:03:35

Q. It's shown in Figure 14, and discussed in a couple of other places. 10:03:37 10:03:39

A. Ah, yeah, yeah, this is the device which is supposed to be connecting directly to the front side bus of the processor, right? 10:03:50 10:03:51 10:03:53

Q. Right. 10:03:55

A. So, the idea is going in the exact direction because for a network like SCI, PCI was an infinitely slow bus, right? SCI was designed to run at speeds of a gigabyte per second, which at that time was unbelievably past. Today we do this very comfortably where PCI 32-bit 33 megahertz is 120 megabytes per second, it's roughly a factor eight slower. So, of course, there was some interest to do away with this limitation and connect more directly to the front side bus. But to my knowledge now, this is mentioned on page 16, let me just see, do you 10:03:56 10:03:59 10:04:08 10:04:13 10:04:15 10:04:19 10:04:26 10:04:31 10:04:35 10:04:38 10:04:40 10:04:42

remember which section it was? 10:04:45

Q. I was just asking a simple 10:04:46

question whether you worked on the PRO-SCI 10:04:50

device, not how it worked. 10:04:52

A. My point is I don't believe it 10:04:54

existed at that time, it was only mentioned here 10:04:56

as work in progress, to come soon, but this is 10:04:58

why I wanted to check. Consequently I couldn't 10:05:01

have worked on it anyway. It doesn't say much 10:05:03

about it here. 10:05:14

Q. Okay. A couple of quick questions 10:05:15

in the time I have remaining here. 10:05:17

We talked yesterday about the CERN 10:05:19

library. Do you know whether the CERN library in 10:05:21

1996 had a searchable database that was on the 10:05:27

internet for people to use to see what was in the 10:05:32

CERN library? 10:05:34

A. I don't know that. 10:05:35

Q. Okay. And do you know whether the 10:05:36

CERN library participated in repository exchange 10:05:39

programs with other libraries where other 10:05:46

libraries could borrow books from CERN and vice 10:05:49

versa in the 1996 timeframe? 10:05:53

A. I'm unaware of that. There are 10:06:00

only some very, very few local universities in 10:06:05

the area, the next is Lausanne which is 80 kilometers away. And copyright-wise I would expect some hefty problems if an international organization, which is basically having complete diplomatic immunity, is loaning a book to a university in another country, because this is what you basically have here. But, I mean, I don't know whether that was the practice. I certainly never tried to loan a book or a publication from CERN, I would only use it from my university library which would be any way more convenient. 10:06:07 10:06:11 10:06:17 10:06:20 10:06:23 10:06:28 10:06:30 10:06:33 10:06:35 10:06:38 10:06:43 10:06:47

Q. One quick follow-up question on encoding. Is taking something that's parallel and converting it into some serial format, does that meet your definition of encoded? 10:06:47 10:06:50 10:06:55 10:06:59

A. I believe I -- 10:07:02

MR. DAVIS: Object to form. 10:07:03

THE WITNESS: -- wrote that and I believe that's -- let me just check. 10:07:05 10:07:06

BY MR. BUROKER: 10:07:09

Q. I think it is. 10:07:09

A. 78 on '814, right? 10:07:11

Q. Yeah. 10:07:14

A. "Therefore the [broadest 10:07:27

reasonable interpretation] of 'encode' in light of the specification ..." 10:07:29 10:07:30

-- this is why I like to refer to the particular patent -- 10:07:31 10:07:33

"... is 'a reversible operation that turns signals into bits, packetizes bits into a specified size packet, or orders bits onto one or more serial transmission lines'". 10:07:33 10:07:35 10:07:39 10:07:41

So then the answer to your question is yes, it meets that statement specification. 10:07:43 10:07:45

MR. BUROKER: Respectful of our agreement, I am out of time. I think you have got your time, I will pass over the witness to your counsel. 10:07:52 10:07:54 10:07:56 10:07:58

MR. DAVIS: All right, can we go off the record for a minute? 10:08:00 10:08:02

(Brief recess 10:08 a.m. - 10:18 a.m.) 10:18:51

EXAMINATION 10:18:56

BY MR. DAVIS: 10:18:58

Q. Dr. Lindenstruth, thank you for being here today. This is the portion of your deposition that's called redirect. I have four hours under the agreement between the parties, but I hope it won't take me that long. 10:18:59 10:19:00 10:19:02 10:19:05 10:19:07

The first thing. Mr. Buroker asked you 10:19:14

a lot of questions today and yesterday about your declaration. Aside from a few of the typos that you mentioned, you still stand behind the opinions as set out in your declarations of the '814 and '873 IPRs; is that correct? 10:19:17 10:19:19 10:19:23 10:19:27 10:19:31

A. Yes, I do. Yeah. 10:19:37

Q. And yesterday Mr. Buroker asked you about your background, you remember that? 10:19:38 10:19:42

A. I remember that, yeah. 10:19:44

Q. Do you remember the discussion about LHC, the acronym? 10:19:45 10:19:52

A. Yes. 10:19:54

Q. I don't know that the full long form of that was ever discussed. Could you tell me what LHC stands for? 10:19:55 10:19:58 10:20:03

A. LHC stands for Large Hadron Collider, which is the accelerator built at CERN to which the experiments are connected. 10:20:07 10:20:10 10:20:14

Q. And, let's see, you were asked some questions about the RD24 status report, which we've been referring to as the Bogaerts reference, right? 10:20:26 10:20:29 10:20:35 10:20:37

A. That's correct. 10:20:39

Q. And that's EMC Exhibit 1011 in the '814 Patent IPR; is that correct? 10:20:40 10:20:45

A. Yes, I think so. 10:20:50

Q. Now, I think you mentioned that 10:20:51

not all of the functionality disclosed in the 10:20:59

Bogaerts reference had been implemented at the 10:21:02

time it was presented at the RD24 Committee; is 10:21:04

that correct? 10:21:07

MR. BUROKER: Objection to form. 10:21:09

BY MR. DAVIS: 10:21:11

Q. Let me re-ask that in a less 10:21:11

leading way. 10:21:14

Are you aware if all of the 10:21:16

functionality disclosed in the RD24 status report 10:21:18

had been implemented at the time it was presented 10:21:21

to the RD24 Committee. 10:21:24

MR. BUROKER: Objection to form. 10:21:29

THE WITNESS: I mean this is a status 10:21:30

report of ongoing work and one has to understand 10:21:32

that there have been quite a few of such research 10:21:37

and development projects for different 10:21:41

technologies and several of them were in direct 10:21:43

competition, so this is not only a status report 10:21:45

of ongoing work but it also says how useful could 10:21:48

this be if done in its final form, where the 10:21:52

final form would end up being many, many years 10:21:56

ahead in time, right? I mean we're talking here 10:21:58

1996 and at that time I believe the scheduled operation for the LHC was 2005. Nine years in the future. And even 2005 it didn't happen. 10:22:01 10:22:04 10:22:07

So there is some content in here which is, so to say, a sketch what could happen, and there is in particular for the PCI-SCI adapter quite a bit of functionality which did not yet exist. So, for instance, on page 10 there is a list of features which were implemented but there are also features which are not yet implemented and that includes the transparent transactions, which is exactly that functionality we have been discussing quite a bit of also this morning. I should probably mention that in this particular context, in particular the functionality to make such an interface perform at least at some level, ended up in me submitting another patent which was approved later. 10:22:13 10:22:17 10:22:21 10:22:30 10:22:32 10:22:39 10:22:44 10:22:47 10:22:50 10:22:53 10:22:59 10:23:01 10:23:05 10:23:08 10:23:14

So there is some highly complex functionality in here and not everything is either disclosed in here or even yet done. 10:23:16 10:23:18 10:23:20

BY MR. DAVIS: 10:23:26

Q. Is the disclosure in your opinion in the Bogaerts reference enough to enable a person of ordinary skill in the art to create 10:23:28 10:23:31 10:23:34

a system such as that described in the '814 Patent, claim 31? 10:23:38 10:23:44

MR. BUROKER: Objection; outside the scope of his declaration, outside the scope of cross. Go ahead. 10:23:45 10:23:47 10:23:48

THE WITNESS: I mean claim 31, '814. This is the wrong document. Let me just pull this out one more time. 10:23:53 10:23:58 10:24:05

Right, I mean, this is the method claim for operating a computer system where an ACM inserted into a console, with a microprocessor, various LVDS channels, the peripheral bridges and including the security program which we haven't discussed much about. 10:24:17 10:24:20 10:24:24 10:24:30 10:24:37 10:24:39

So in order to put such a system together, I mean I have made the statement that SCI would not be the technology which would be useful to do that at all. So consequently a person of ordinary skill in the art couldn't do it at all. And, second, one has to understand that what we are discussing here is basically the context of massive parallel high-performance computer systems, which is not part of the standard curriculum of a bachelor in computer science. I believe I said something like that 10:24:41 10:24:44 10:24:54 10:24:56 10:24:59 10:25:01 10:25:05 10:25:09 10:25:13 10:25:17 10:25:21

earlier, too. 10:25:23

BY MR. DAVIS: 10:25:38

Q. You mentioned that the disclosure 10:25:38

in the Horst reference yesterday was extremely 10:25:40

high-level in response to Mr. Buroker's 10:25:44

questions; is that correct? 10:25:47

A. I believe that's correct, yes. 10:25:48

Q. Is the disclosure in the Horst 10:25:51

reference sufficient to allow a person of 10:25:53

ordinary skill in the art to create the system 10:25:58

disclosed in the Horst reference? 10:26:01

MR. BUROKER: Objection to form, 10:26:04

objection outside the scope of his declaration 10:26:06

and outside the scope of cross. 10:26:09

THE WITNESS: You just asked whether 10:26:17

a person of ordinary skill in the art would be 10:26:18

able to reproduce Horst itself, not in light of 10:26:20

the patents, correct? 10:26:23

BY MR. DAVIS: 10:26:25

Q. Correct. 10:26:26

A. I mean same argument, this is 10:26:33

another variant of a massive parallel computer 10:26:35

system. The network is more simple than SCI 10:26:40

because it doesn't have cache coherency 10:26:43

functionality yet, it is a complex network of 10:26:46

which only some very little sketchy details are disclosed in here. So to build the TNet system as disclosed here there is certainly by far not enough information. To build something like TNet would certainly require a lot more than one person of ordinary skill in the art, one would require different specializations, you have very high-speed physical layers inside the network, you have a complex network structure, there are routers shown here, routing functionality, there is redundant signal paths in here. That opens the entire context of a sequential consistency for computers. What happens if a packet sent later bypasses a packet which is in congestion in another path and so forth? 10:26:49 10:26:53 10:26:59 10:27:01 10:27:06 10:27:09 10:27:12 10:27:16 10:27:18 10:27:22 10:27:27 10:27:29 10:27:37 10:27:39 10:27:43

So, I read this Horst reference as a document which shows the overall concept of TNet for a person to understand that there is some substance behind it, but it's certainly not enough to build it and I would expect that Tandem would never have allowed Horst to do that because it's a proprietary product which they would want to use for themselves and sell and wouldn't want to have anybody copy it. 10:27:47 10:27:53 10:27:57 10:28:00 10:28:03 10:28:07 10:28:10 10:28:12 10:28:15

/// 10:28:16

BY MR. DAVIS: 10:28:16

Q. Do you remember when Mr. Buroker 10:28:17

asked you yesterday if a single PCI bus 10:28:19

transaction was sufficient to meet the terms of 10:28:23

claim 24's limitation. 10:28:27

MR. BUROKER: Objection to form. 10:28:29

THE WITNESS: I am not exactly sure, 10:28:30

there have been so many questions. Yes, could 10:28:32

well be. 10:28:37

BY MR. DAVIS: 10:28:40

Q. So I have a question. Does the 10:28:40

Horst reference -- which is Exhibit 1009, I 10:28:42

believe, in the '814 IPR -- disclose even a 10:28:51

single PCI bus transaction across the TNet system 10:28:57

area network? 10:29:00

A. It does not disclose this. 10:29:01

MR. BUROKER: I'm sorry, objection; 10:29:04

form to that question and the answer. Sorry, I 10:29:06

wasn't quick enough. Go ahead. 10:29:09

Just as you had to wait for your 10:29:16

counsel, I'm in the reverse role so just give me 10:29:17

a quick second, if you would. 10:29:20

THE WITNESS: I apologize. 10:29:22

MR. BUROKER: It is my fault, I wasn't 10:29:23

very quick that time. 10:29:25

THE WITNESS: And I shouldn't shoot too fast, as I didn't before. 10:29:26 10:29:29

BY MR. DAVIS: 10:29:35

Q. In reference to claim 24 of the '814 Patent, Mr. Buroker asked you yesterday about the difference between encoded data of peripheral component interconnect bus transaction in the first limitation, and address and data bits of PCI bus transaction in the later limitations of claim 24. 10:29:35 10:29:38 10:29:51 10:29:54 10:29:58 10:30:03 10:30:07

A. Yes. 10:30:11

Q. Does your opinion that a northbridge to communicate address and data bits of a PCI transaction depend on how you interpret encoded data of PCI bus transaction in the first limitation? 10:30:11 10:30:16 10:30:18 10:30:24 10:30:28

MR. BUROKER: Objection; form. 10:30:30

THE WITNESS: I'm not sure I understand the question. 10:30:39 10:30:41

BY MR. DAVIS: 10:30:42

Q. Okay. 10:30:42

A. We have "transmit encoded data" in the first part of the claim and then later we have "to communicate address and data bits of PCI bus transaction". Since it's in the same claim 10:30:43 10:30:45 10:30:48 10:30:52

I would assume that they are encoded. 10:30:54

Q. I guess I'm going after a slightly 10:31:00
different question. Whether or not encoded data 10:31:02
of PCI component bus or peripheral component 10:31:07
interconnect bus transaction also includes the 10:31:12
address of a PCI bus transaction doesn't depend 10:31:15
on whether address and data bits of a PCI bus 10:31:20
transaction includes PCI address information, 10:31:25
does it? 10:31:27

MR. BUROKER: Objection to form. 10:31:28

THE WITNESS: I would agree. 10:31:31

BY MR. DAVIS: 10:31:47

Q. So, in your opinion, the fact that 10:31:48
a northbridge to communicate address and data 10:31:52
bits of a PCI bus transaction -- strike that. 10:31:54
I'll come back to that. 10:32:05

Let's turn to paragraph 114 of your '814 10:32:20
declaration. For the record that's Exhibit 2021 10:32:23
in IPR 2014-01469. And when I've been referring 10:32:32
to the '814 IPR I've been referring to that IPR 10:32:40
number. 10:32:43

So on page 77, Mr. Buroker asked you 10:32:58
about a sentence starting at the top of the page: 10:33:02

"... they require the address and data 10:33:13
phases of a PCI bus transaction, which include 10:33:16

the PCI address bus command information during the address phase ... and the PCI data and byte enables during the data phases ..." 10:33:19 10:33:22 10:33:26

Do you see that? 10:33:29

A. Yeah. 10:33:30

Q. I'd like to point you back to page 34 of your declaration. You see at the top there, there's a section that's headed "2.2.2. Address and Data Pins"? 10:33:31 10:33:37 10:33:44 10:33:49

A. Page 32. 10:33:55

Q. 34, sorry. 10:33:56

A. Yes. This is an excerpt from the PCI specification. 10:33:59 10:34:04

Q. So, do you see where it says, "AD [31::00]"? 10:34:07 10:34:12

A. Yeah. 10:34:16

Q. Can you read the second sentence starting with "A" on the first line? 10:34:16 10:34:19

A. "For I/O, this is a byte address; for configuration in memory, it is a [double] word address. During the data phases [address data] [7::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb)." 10:34:23 10:34:24 10:34:27 10:34:32 10:34:35 10:34:38

Q. Okay, so I was talking about the 10:34:40

paragraph above it. The first sentence is: 10:34:41

"*Address* and *Data* are multiplexed ..." 10:34:45

A. "*Address* and *Data* are multiplexed 10:34:47

on the same PCI pins. A bus transaction consists 10:34:47

of an address phase followed by one or more data 10:34:51

phases." 10:34:54

Q. And do you agree with that 10:34:54

statement? 10:34:56

A. Yeah, I mean this is the standard. 10:34:56

Q. Can you turn to the PCI local bus 10:34:59

specification which is Exhibit 2001 I think in 10:35:05

both IPRs. 10:35:07

A. Yes, I have it. 10:35:21

Q. This is page 25, go to page 25 of 10:35:21

the exhibit, which is page 9 of the document. 10:35:26

A. Yes. I have it. 10:35:29

Q. Does the section 2.2.2 there 10:35:30

accurately reflect the section excised on page 34 10:35:35

of your declaration? 10:35:40

A. Yeah, I copied that part. 10:35:41

Q. Can you read the 10:35:43

paragraph starting after "C/BE[3::0]"? 10:35:47

A. The third line of the third 10:35:55

paragraph, right? 10:35:56

I mean, I would read it as: 10:35:59

"[Command slash byte enable three through zero] define the bus command (refer to Section 3.1 for bus command definitions). During the data phase [command slash byte enable] are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. [Command byte enable 0 applies to byte 0 [the least significant byte] and [command byte enable] 3 applies to byte 3 the [most significant byte]." 10:36:02 10:36:04 10:36:08 10:36:13 10:36:17 10:36:20 10:36:24 10:36:34 10:36:35 10:36:39

Q. Thank you, and if you turn back to page 77, paragraph 114 of your declaration, the '814 declaration. I don't know if you remember, but Mr. Buroker asked you about the citation to the PCI specification in that portion of your declaration yesterday. Do you remember that? 10:36:41 10:36:43 10:36:49 10:36:59 10:37:02 10:37:07

A. I remember. 10:37:08

Q. Does the section of the PCI specification you just read report your construction of the PCI bus transaction as PCI address and bus command information during the address phase and PCI data and byte enables during the data phases? 10:37:09 10:37:12 10:37:15 10:37:20 10:37:22 10:37:25

MR. BUROKER: Objection; form. 10:37:26

THE WITNESS: It does. It does. 10:37:29

BY MR. DAVIS: 10:38:10

Q. Do you remember yesterday when 10:38:10

Mr. Buroker asked you about the claim 10:38:11

construction standards you applied when forming 10:38:13

the opinions in your declaration? 10:38:15

A. I remember this discussion. 10:38:16

Q. I think there was some discussion 10:38:22

about paragraph 20. 10:38:24

A. Yes, I have it in front of me. 10:38:38

Q. Okay, so I just want to make sure, 10:38:40

because I got confused yesterday, did you apply 10:38:44

the broadest reasonable interpretation of claims 10:38:52

in light of the specification when you construed 10:38:55

terms of the patents? 10:39:04

A. Yes, I did. 10:39:06

Q. Mr. Buroker also discussed with 10:39:25

you the meaning of "PCI bus transaction" as 10:39:27

a "PCI standard bus transaction". You remember 10:39:32

that? 10:39:34

A. I remember that. 10:39:34

Q. The definition you set out in 10:39:35

paragraph 114, is that the definition you applied 10:39:51

in performing the analysis set out in your 10:39:54

declaration? 10:39:58

A. This is correct. 10:39:59

Q. Mr. Buroker also asked you about the construction of "encoded", I believe; is that correct? 10:40:00 10:40:14 10:40:20

A. This is correct. 10:40:20

Q. And you still agree or do you still agree with the claim construction you set out in paragraph 120 of your declaration? 10:40:21 10:40:36 10:40:38

A. Yes, absolutely I do. I believe I already read it, and the preceding paragraphs outline the reasoning for this conclusion. 10:40:46 10:40:48 10:40:53

Q. And yesterday Mr. Buroker asked you some hypotheticals about specific cases of schematics shown in the Horst reference. Do you remember that? 10:40:58 10:41:01 10:41:12 10:41:16

MR. BUROKER: Objection to form, mischaracterizes. 10:41:17 10:41:19

THE WITNESS: I sure do that. 10:41:22

BY MR. DAVIS: 10:41:24

Q. Did Mr. Buroker ask you to discuss a system in Horst that only had one CPU memory block and only a PCI interface? 10:41:25 10:41:27 10:41:30

A. Yes, I remember that. 10:41:34

Q. Is that schematic shown anywhere in Horst? 10:41:35 10:41:40

MR. BUROKER: Objection to form. 10:41:41

THE WITNESS: It is not shown. 10:41:47

BY MR. DAVIS: 10:41:48

Q. Regardless of how the systems in 10:41:49

Horst were set together, would that change the 10:41:54

operation of the TNet system area network as 10:41:56

disclosed in Horst? 10:41:59

MR. BUROKER: Objection to form. 10:42:01

THE WITNESS: The TNet as set out here 10:42:04

has a defined functionality set and that is 10:42:05

independent of the number of nodes connected to 10:42:08

it so, no, it would not change. 10:42:12

BY MR. DAVIS: 10:42:25

Q. And is it true that even under 10:42:25

Mr. Buroker's hypothetical situation, that a PCI 10:42:27

standard address would never be transmitted over 10:42:31

the TNet system network? 10:42:35

MR. BUROKER: Objection; form. 10:42:37

THE WITNESS: I mean, according to what 10:42:39

is laid out in the reference we have here, the 10:42:40

Horst reference, this is correct. There are TNet 10:42:45

addresses and they are virtual addresses they are 10:42:49

translated addresses and it is spelt out in this 10:42:52

document. 10:42:54

BY MR. DAVIS: 10:43:09

Q. Is the same also true for the 10:43:09

systems disclosed in the Bogaerts reference? 10:43:12
That a PCI standard address would never be 10:43:17
transmitted over the SCI ring? 10:43:26
MR. BUROKER: Objection to form. 10:43:28
THE WITNESS: The arguments go 10:43:29
basically along the same lines, and the answer is 10:43:31
yes. It's a different address scheme, there's 10:43:33
more bits, but the principle is the same. 10:43:36
BY MR. DAVIS: 10:43:43
Q. Remember when Mr. Buroker asked 10:43:44
you about the IBM dictionary, Exhibit 2024? 10:43:45
A. Yes. 10:43:50
Q. And I believe he asked you 10:44:17
questions about code? 10:44:19
A. Yeah. 10:44:23
Q. Which is on page 4 of the exhibit, 10:44:23
page 111 of the document. 10:44:25
A. Correct. 10:44:32
Q. Can you tell me what the last 10:44:32
sub-definition in parentheses number 13 at the 10:44:36
bottom of code says? 10:44:42
MR. BUROKER: Objection outside the 10:44:44
scope of his declaration and cross. 10:44:46
THE WITNESS: It says: 10:44:52
"Pseudonym for encode." 10:44:53

BY MR. DAVIS: 10:45:15

Q. Do you remember when Mr. Buroker 10:45:15

asked you about IEEE 1394 FireWire yesterday? 10:45:17

A. Yes, I do remember. 10:45:20

Q. Is FireWire a communications 10:45:22

protocol? 10:45:30

A. Yes, it is. 10:45:30

Q. Is FireWire the same as PCI? 10:45:31

A. Absolutely not. I didn't want to 10:45:35

say much yesterday, in particular because I 10:45:44

hadn't available the FireWire standard, I pulled 10:45:47

it yesterday night. It is a 900-page document, 10:45:52

obviously I did not read everything, but I looked 10:45:55

over it to refresh my mind and I believe the 10:45:57

discussion was about the signalling, the physical 10:46:00

signalling in FireWire as opposed to LVDS or as 10:46:03

in contrast to LVDS. 10:46:07

Q. Do you remember when Mr. Buroker 10:46:26

asked you yesterday about a paper by Hans Muller, 10:46:29

"SCI implementation study for LHCb Data 10:46:35

Acquisition"? I think he marked it as 10:46:40

Exhibit 1027 in both. 10:46:42

A. I have it in front of me. I 10:46:45

remember. 10:46:48

Q. Is this document referenced 10:46:50

anywhere in your declaration? 10:46:52

A. It is not, I have seen it the 10:46:54

first time yesterday. 10:46:55

Q. So none of the opinions in your 10:46:57

declaration relate to this document in any way; 10:47:00

is that correct? 10:47:03

A. This is correct. 10:47:04

Q. I'd like to take you to the 10:47:08

references section on page 19 on the document. 10:47:11

If you look at bracket 6 there, it says: 10:47:22

"RD24 status report 1996." 10:47:25

Do you see that? 10:47:27

A. Yes, I see that. 10:47:29

Q. Is that a cite to the CERN library 10:47:30

at the end there? 10:47:36

A. No, this is -- and I believe I 10:47:37

said this or wrote this also in my declaration -- 10:47:38

this is the sunshine server which is one of the, 10:47:42

I believe, two machines which were used in the 10:47:47

RD24 project operated by the project leader of 10:47:50

the RD24, which was Hans Müller. 10:47:53

Q. And can you read the last portion 10:47:57

of that address after the slash, the last slash? 10:48:00

A. You mean "/PCI"? 10:48:05

Q. No, "/rd24.html", do you see that? 10:48:07

A. I'm sorry, I'm sorry, I was on the wrong line. You mean "http://"? 10:48:15 10:48:17

Q. Yes, so if you go to the end of the sunshine.cern.ch:8080/RD24, it says "RD24/rd24.html". 10:48:26 10:48:32 10:48:33

A. It does say that. 10:48:36

Q. Now, Mr. Buroker also asked you about a Butler declaration from the Internet Archives; is that right? 10:48:37 10:48:40 10:48:44

A. Correct. 10:48:46

Q. And the RD24 status report which is similar to the Bogaerts document, which is Exhibit 1001 in the '814 IPR, the web pages for the eight pieces of that end in RD2496_[number].ps"; is that correct? 10:48:47 10:48:52 10:48:57 10:49:05 10:49:12

A. Yes. 10:49:16

MR. BUROKER: Objection; foundation, form. 10:49:17 10:49:18

BY MR. DAVIS: 10:49:24

Q. So that's a different web address that you see in -- or is that a different web address that you see in number 6 there in the references at the end of Exhibit 1027? 10:49:24 10:49:26 10:49:30 10:49:32

MR. BUROKER: Objection; form. 10:49:35

THE WITNESS: It is different, yes. 10:49:38

BY MR. DAVIS: 10:49:52

Q. Does the RD2496_[number].ps 10:49:52

address appear anywhere in Exhibit '27 to your 10:49:59

knowledge? 10:50:02

A. Sorry, the RD24_ what? 10:50:02

Q. The web address for the postscript 10:50:11

files in the Butler declaration, does that appear 10:50:13

anywhere in Exhibit 1027 to your knowledge? 10:50:16

A. I am not seeing it anywhere. 10:50:23

Q. Is there anything in the 10:50:33

Exhibit 1027 which indicates it was a final 10:50:36

version? 10:50:42

A. There is no -- not in -- 10:50:53

MR. BUROKER: Objection; form. I'm not 10:50:57

sure what the "it" is. Go ahead. 10:50:59

THE WITNESS: I mean basically this is 10:51:03

a document which is dated. This is all there is 10:51:05

to it. There is no kind of record. I mean it 10:51:09

does say "LHCb note", which means it could be 10:51:19

that this is a final note, it could be that this 10:51:23

is something in preparation. I cannot tell. 10:51:26

BY MR. DAVIS: 10:51:32

Q. And the author, Hans Müller, he is 10:51:32

also an author of the RD24 status report; is that 10:51:35

correct? 10:51:38

A. This is correct, yeah. 10:51:39

Q. I want to come back to "encode". 10:52:27

Mr. Buroker asked you about "encode" in the 10:52:29

patent a few times, and your construction of 10:52:32

that. Do you remember? 10:52:35

A. I remember. 10:52:37

Q. And he also asked you about 10:52:38

address translation a number of times; is that 10:52:43

correct? 10:52:45

A. That is correct. 10:52:46

MR. BUROKER: Objection to form. 10:52:46

BY MR. DAVIS: 10:52:52

Q. Is it your opinion that address 10:52:52

translation is not encoding at least because 10:52:55

address translation is not reversible? 10:52:59

MR. BUROKER: Objection; leading. 10:53:01

Objection to form. 10:53:02

THE WITNESS: I believe I am saying 10:53:05

this rather explicit in my declaration and the 10:53:08

answer is yes. Let me just -- 10:53:12

BY MR. DAVIS: 10:53:16

Q. Let me ask a slightly different 10:53:17

question. Is address translation reversible? 10:53:18

A. It is not. 10:53:22

MR. BUROKER: Objection to form. 10:53:23

THE WITNESS: And for that we do cite the textbook by Dave Patterson and John Hennessy. I am just trying to find it in here real quick. 10:53:25 10:53:28 10:53:35

I mean there is, starting at section 39, a whole discussion about that and the reference is cited. The virtual-to-physical address translation is not reversible and therefore cannot be considered to be encoding, and this is one of the reasons why it's called address translation and not address encoding. 10:54:58 10:55:00 10:55:05 10:55:10 10:55:12 10:55:17 10:55:19

BY MR. DAVIS: 10:55:24

Q. So we've been discussing encoding and PCI bus transaction in the context of '814 IPR. Are your opinions about the constructions of those claim terms the same in your '873 IPR patent direction, which is IPR2014-01462? 10:55:24 10:55:27 10:55:31 10:55:35 10:55:46

A. I mean I said before what claim construction is to be used in both declarations for the term "encoded" -- you asked for "encoded" right? 10:55:54 10:55:57 10:56:06 10:56:11

Q. Well, for both "PCI" and "encoded". Let me see where they're set out here and I'll ask you. Page 71 of your '873 declaration. 10:56:12 10:56:18 10:56:21 10:56:31

A. In case of the '814 declaration it 10:56:52

is paragraph 120, saying: 10:57:00

"... the [broadest reasonable 10:57:03

interpretation] of 'encode' in light of the 10:57:05

specification is 'a reversible operation that 10:57:06

turns signals into bit, packetizes bits into 10:57:10

a specified size packet, or orders bits onto one 10:57:13

or more serial transmission lines'". 10:57:16

And in case of the '873 Patent it is 10:57:21

the same. 10:57:25

Q. And it is set out at paragraph 125 10:57:27

of your declaration in the '873 IPR? 10:57:30

A. That is correct, that's where it 10:57:34

says. 10:57:35

Q. And if you look at page 72, 10:57:38

paragraph 119 of your '873 IPR declaration, about 10:57:40

five lines up from the bottom in paragraph 119 10:57:59

there's a semi-colon and then: 10:58:02

"... they require the address and data 10:58:05

phases of a PCI bus transaction ..." 10:58:07

Do you see that? 10:58:11

A. On page 72? 10:58:12

Q. Yes. 10:58:13

A. No, I don't see that, I'm 10:58:25

confused. On page 72, '873. Yes, now I see it. 10:58:26

Q. Does the portion of the PCI 10:58:49

specification at page 25 of the exhibit that we discussed earlier support your construction of "PCI bus transaction" as set out in your '873 Patent declaration? 10:58:54 10:58:59 10:59:05 10:59:12

MR. BUROKER: Objection; outside the scope of his declaration. 10:59:15 10:59:17

THE WITNESS: It certainly does, and it is rather clearly spelt out here and based then on my experience working with PCI certainly it does. 10:59:26 10:59:31 10:59:37 10:59:41

BY MR. DAVIS: 10:59:42

Q. Okay, and could you turn to page 33 of your '873 declaration? 10:59:42 10:59:44

A. And here is the copy. 10:59:56

Q. Could you elaborate on that? A copy of what? 10:59:58 11:00:00

A. This is the copy of the section 2.2.2 of the PCI local bus specification which outlines clearly the functionality of the major control signals used in PCI to basically define the bus state, to define the bus commands executed and the validity of the data, namely which is coded by so-called command/byte enable signals, but it also shows the flow control signals, initiator ready and target ready and the 11:00:01 11:00:04 11:00:11 11:00:17 11:00:21 11:00:24 11:00:26 11:00:33 11:00:36

frame signal which basically defines the packet length. And this is why this is nicely and concisely described here, although there is many more details in the specification I put it into the declaration for clarity. 11:00:39 11:00:41 11:00:44 11:00:47 11:00:49

MR. DAVIS: Can we go off the record? 11:00:53

(Brief recess taken 11:01 a.m. - 11:04 a.m.) 11:00:55

MR DAVIS: So, thank you, Dr. Lindenstruth. I'll pass you back to Mr. Buroker for recross. 11:04:38 11:04:39 11:04:42

EXAMINATION 11:04:46

BY MR. BUROKER: 11:04:47

Q. Dr. Lindenstruth, on redirect, you were asked whether or not you recalled the discussion we had yesterday regarding IEEE 1394, which is also sometimes called FireWire. 11:04:48 11:04:51 11:04:56 11:05:00

A. Yes. 11:05:04

Q. Do you remember that? 11:05:04

A. I remember that. 11:05:06

Q. And you said that you determined that it is a communication protocol; is that correct? 11:05:06 11:05:10 11:05:12

A. This is correct. 11:05:13

Q. Do you recall yesterday it came up in the context of my question from column 22 of 11:05:14 11:05:16

the '814 Patent in which IEEE 1394 is referenced. 11:05:21
If you could turn to that, please. It's 11:05:27
column 22 lines 7 to 8. 11:05:34
MR. DAVIS: Objection; outside the 11:05:44
scope of redirect. 11:05:46
THE WITNESS: Yes, I'm back at that 11:05:48
page. 11:05:50
BY MR. BUROKER: 11:05:52
Q. Did you determine whether IEEE 11:05:53
1394 is a form low-voltage differential 11:05:56
signalling communication? 11:06:05
A. That was one of the reasons I 11:06:05
looked at that. 11:06:07
Q. And what -- oh sorry? 11:06:08
A. Within these 900 pages of this 11:06:15
document, there is a rather large number of 11:06:17
connectors and cable specified and for many of 11:06:20
those there are specific voltage levels for 11:06:23
communication set forth which are having slight 11:06:27
variations with respect to voltage levels and 11:06:33
currents being used on the signals, but they are 11:06:36
very well within the kind of context and scope of 11:06:39
LVDS. So, for example, LVDS has a midpoint of 11:06:46
1.2 volt, I believe they are slightly higher. 11:06:50
LVDS has a slightly smaller voltage swing than 11:06:52

what is outlined there and there may be also different impedances assumed because there are different cables being involved. LVDS 1596.3 was defined as an abstract standard for any kind of low-voltage differential signalling, while here it is the physical signalling for this particular communication standard which includes all the definitions of connectors on that as well. 11:06:58 11:07:04 11:07:07 11:07:20 11:07:23 11:07:25 11:07:29 11:07:31

Q. And so are you saying that IEEE 1394 is a form of LVDS -- 11:07:34 11:07:37

MR. DAVIS: Objection to form. 11:07:47

BY MR. BUROKER: 11:07:49

Q. -- communication? 11:07:50

MR. DAVIS: Objection to form and outside the scope of redirect. 11:07:50 11:07:52

THE WITNESS: No, 1394 is a complete standard for the complete protocol and everything, including what we usually call physical signalling, right? Where in SCI the physical signalling for LVDS was made a separate substandard 1594.3. This is all included in FireWire here in 1394. Therefore it is more than just a physical signalling but it is included. 11:07:54 11:07:58 11:08:01 11:08:04 11:08:09 11:08:15 11:08:18 11:08:26

BY MR. BUROKER: 11:08:28

Q. You said you looked at a standard 11:08:28

last night. Was that a current standard for 1394 or one that was in existence in 1998 when the '814 Patent was filed. 11:08:30 11:08:34 11:08:39

MR. DAVIS: Objection to form. 11:08:43

BY MR. BUROKER: 11:08:45

Q. Go ahead. 11:08:45

A. This is a good question, the original 1394 standard was superseded and I looked it the current standard. The old one I couldn't get. So one has to take this with a little bit of a grain of salt but, on the other hand, since there is quite a bit of interoperability between these different versions would assume there to be -- well, no, I don't want to make any assumptions here, no, I'm not going to because that wouldn't be right, I'm still under oath. 11:08:46 11:08:48 11:08:53 11:08:55 11:08:57 11:09:00 11:09:14 11:09:16 11:09:19 11:09:21 11:09:23

Q. So the testimony you gave about low-voltage differential signalling and -- strike that. 11:09:25 11:09:29 11:09:29

The testimony you just gave about IEEE 1394 is based on having read the current version of that standard and not the one that was in place before 1998 when this '814 Patent was filed; is that correct. 11:09:33 11:09:37 11:09:42 11:09:45 11:09:50

A. That is correct. 11:09:51

MR. BUROKER: All right, then I have no 11:09:57

further questions, I thank you for your time. 11:09:59

MR. DAVIS: I'm done, I don't have any 11:10:06

more. 11:10:08

(Volume II of II in the deposition of Volker Lindenstruth was terminated at 11:10 a.m.)

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ACKNOWLEDGEMENT OF DEPONENT

I, VOLKER LINDENSTRUTH, do hereby certify that I have read the foregoing transcript of my testimony taken on 8/28/15, and further certify that it is a true and accurate record of my testimony (with the exception of the correction listed below):

Page	Line	Correction

_____
VOLKER LINDENSTRUTH

SUBSCRIBED AND SWORN TO BEFORE ME

THIS _____ DAY OF _____, 20___.

_____

REPORTER'S CERTIFICATION

UNITED KINGDOM:

I, Audrey Shirley, accredited court reporter, do herby certify that the witness whose deposition is hereinbefore set forth appeared before me in London, United Kingdom on the 28th day of August 2015, at 8:57 a.m.; was duly sworn before the commencement of the deposition; that the testimony was taken down by me using machine shorthand; that all appearances of counsel and participants hereto are noted on the appearance page; and that such deposition is a true, correct, and full record of the proceedings.

I further certify that I am not related to nor employed by any of the parties to this action; that I am not employed by counsel for any of the parties to this action; and that I am in no way interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 28th day of August 2015.

AUDREY SHIRLEY, Court Reporter